What is Claimed is:

[c1] 1. A method of designing an integrated circuit chip, said method comprising:

supplying a chip design;

partitioning elements of said chip design according to similarities in voltage requirements and timing of power states of said elements to create voltage islands;

creating a floorplan of said voltage islands;

assessing said floorplan;

repeating said partitioning and said creating of said floorplan depending upon a result of said assessing process; and

outputting a voltage island specification list.

[c2] 2. The method in claim 1, wherein said elements comprise logical partitions of said chip design.

[c3] 3. A method in claim 1, wherein said partitioning comprises assessing waveforms of said elements to identify the timing of periods when said elements can be disconnected from a power supply.

[c4] 4. The method in claim 1, wherein said partitioning comprises identifying allowable voltage ranges for each of said elements, wherein said elements comply with timing requirements when operated within said allowable voltage ranges.

[c5] 5. The method in claim 4, wherein said partitioning further comprises grouping said elements according to similarities of local voltage ranges.

[c6] 6. The method in claim 4, wherein said partitioning further comprises evaluating average chip power consumption and chip timing at different voltage combinations for each of said elements, wherein said voltage combinations are selected to be within said voltage ranges of each element.

[c7] 7. The method in claim 6, wherein said partitioning further comprises selecting from said different voltage combinations that have a chip timing that falls within timing requirements of said chip design and that have a smallest average chip power consumption.

[c8] 8. A method of designing an integrated circuit chip, said method comprising:

supplying a chip design;

partitioning elements of said chip design according to similarities in voltage requirements and timing of power states of said elements to create voltage islands; and

outputting a voltage island specification list.

[c9] 9. The method in claim 8, wherein said elements comprise logical partitions of said chip design.

[c10] 10. A method in claim 8, wherein said partitioning comprises assessing waveforms of said elements to identify the timing of periods when said elements can be disconnected from a power supply.

[c11] 11. The method in claim 8, wherein said partitioning comprises identifying allowable voltage ranges for each of said elements, wherein said elements comply with timing requirements when operated within said allowable voltage ranges.

[c12] 12. The method in claim 11, wherein said partitioning further comprises grouping said elements according to similarities of local voltage ranges.

[c13] 13. The method in claim 11, wherein said partitioning further comprises evaluating average chip power consumption and chip timing at different voltage combinations for each of said elements, wherein said voltage combinations are selected to be within said voltage ranges of each element.

[c14] 14. The method in claim 13, wherein said partitioning further comprises selecting from said different voltage combinations that have a chip timing that falls within timing requirements of said chip design and that have a smallest average chip power consumption.

[c15] 15. A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of designing an integrated circuit chip, said method comprising:

supplying a chip design;

partitioning elements of said chip design according to similarities in voltage requirements and timing of power states of said elements to create voltage islands;
creating a floorplan of said voltage islands;
assessing said floorplan;
repeating said partitioning and said creating of said floorplan depending upon a result of said assessing process; and
outputting a voltage island specification list.

[c16] 16. A program storage device in claim 15, wherein said partitioning comprises assessing waveforms of said elements to identify the timing of periods when said elements can be disconnected from a power supply.

[c17] 17. The program storage device in claim 15, wherein said partitioning comprises identifying allowable voltage ranges for each of said elements, wherein said elements comply with timing requirements when operated within said allowable voltage ranges.

[c18] 18. The program storage device in claim 17, wherein said partitioning further comprises grouping said elements according to similarities of local voltage ranges.

[c19] 19. The program storage device in claim 17, wherein said partitioning further comprises evaluating average chip power consumption and chip timing at different voltage combinations for each of said elements, wherein said voltage combinations are selected to be within said voltage ranges of each element.

[c20] 20. The program storage device in claim 19, wherein said partitioning further comprises selecting from said different voltage combinations that have a chip timing that falls within timing requirements of said chip design and that have a smallest average chip power consumption.

[c21] 21. A method of designing an integrated circuit chip, said method comprising:
supplying a chip design having logical partitions;
grouping said logical partitions according to similarities in voltage requirements and timing of power states of said logical partitions to

create voltage islands;

optimizing said voltage islands by assigning ones of said logical partitions and assigning power sources to said voltage islands that minimize power consumption across said integrated circuit chip; and

outputting a voltage island specification list.

[c22] 22. A method in claim 21, wherein said partitioning comprises assessing waveforms of said logical partitions to identify the timing of periods when said logical partitions can be disconnected from a power supply.

[c23] 23. The method in claim 21, wherein said partitioning comprises identifying allowable voltage ranges for each of said logical partitions, wherein said logical partitions comply with timing requirements when operated within said allowable voltage ranges.

[c24] 24. The method in claim 23, wherein said partitioning further comprises grouping said logical partitions according to similarities and all local voltage ranges.

[c25] 25. The method in claim 23, wherein said partitioning further comprises evaluating average chip power consumption and chip timing at different voltage combinations for each of said logical partitions, wherein said voltage combinations are selected to be within said voltage ranges of each logical partition.

[c26] 26. The method in claim 25, wherein said partitioning further comprises selecting from said different voltage combinations that have a chip timing that falls within timing requirements of said chip design.

[c27] 27. A method of designing an integrated circuit chip, said method comprising:

supplying a chip design having logical partitions;

grouping said logical partitions according to similarities in voltage requirements and timing of power states of said logical partitions to create voltage islands;

optimizing said voltage islands by assigning ones of said logical partitions and assigning

power sources to said voltage islands that minimize power consumption across said integrated circuit chip; and

outputting a voltage island specification list comprising at least one of a power source name, a power source type, minimum voltage level, maximum voltage level, nominal voltage level, switching signal name, switching signal type, power on hours, and steady state on percentage.

[c28] 28. A method in claim 27, wherein said partitioning comprises assessing waveforms of said logical partitions to identify the timing of periods when said logical partitions can be disconnected from a power supply.

[c29] 29. The method in claim 27, wherein said partitioning comprises identifying allowable voltage ranges for each of said logical partitions, wherein said logical partitions comply with timing requirements when operated within said allowable voltage ranges.

[c30] 30. The method in claim 29, wherein said partitioning further comprises grouping said logical partitions according to similarities and all local voltage ranges.

[c31] 31. The method in claim 29, wherein said partitioning further comprises evaluating average chip power consumption and chip timing at different voltage combinations for each of said logical partitions, wherein said voltage combinations are selected to be within said voltage ranges of each logical partition.

[c32] 32. The method in claim 31, wherein said partitioning further comprises selecting from said different voltage combinations that have a chip timing that falls within timing requirements of said chip design.